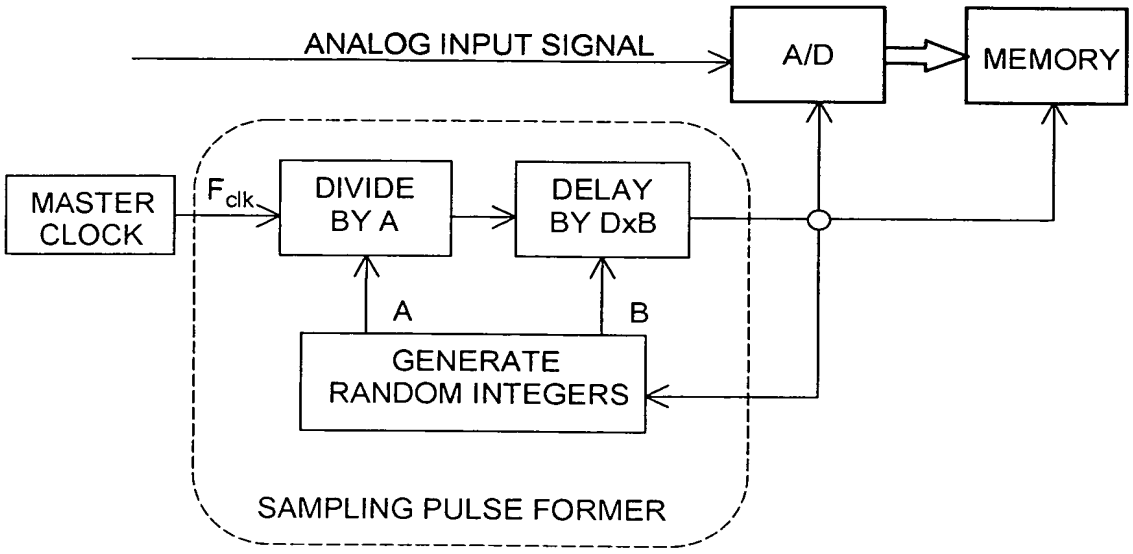

FIG.1. A schematic block diagram of the present invention

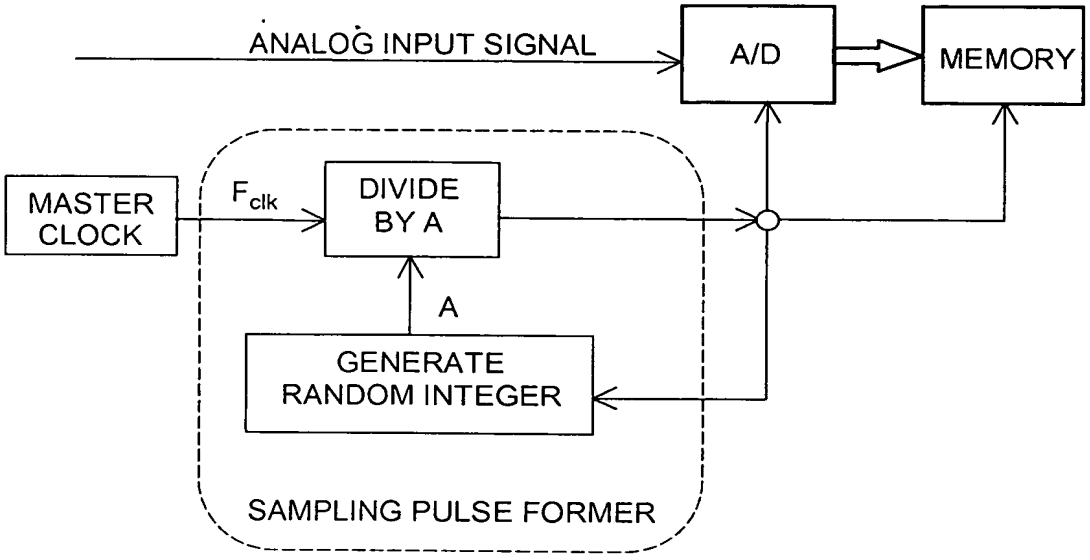

FIG. 2. A schematic block diagram of a priori art circuit

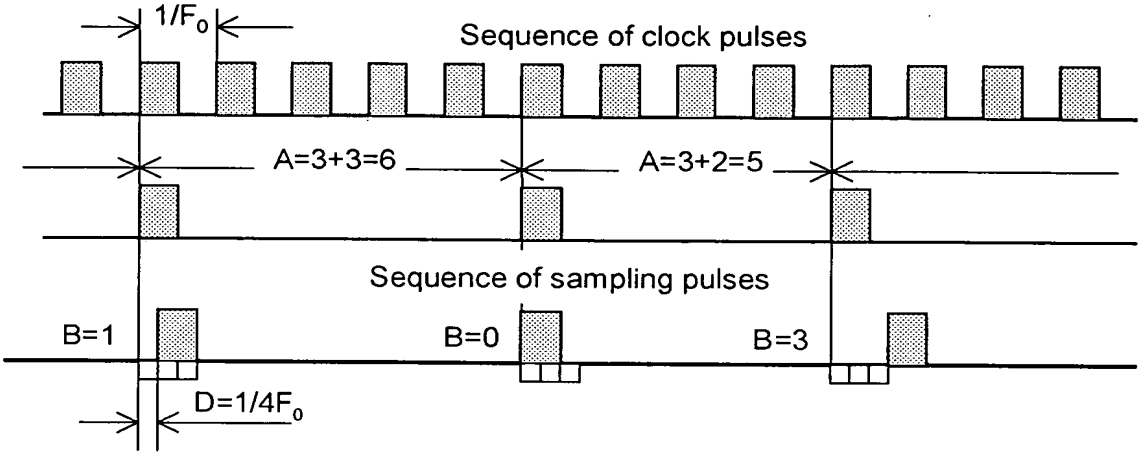

FIG.3. A time diagram showing the manner in which the sampling pulses are formed

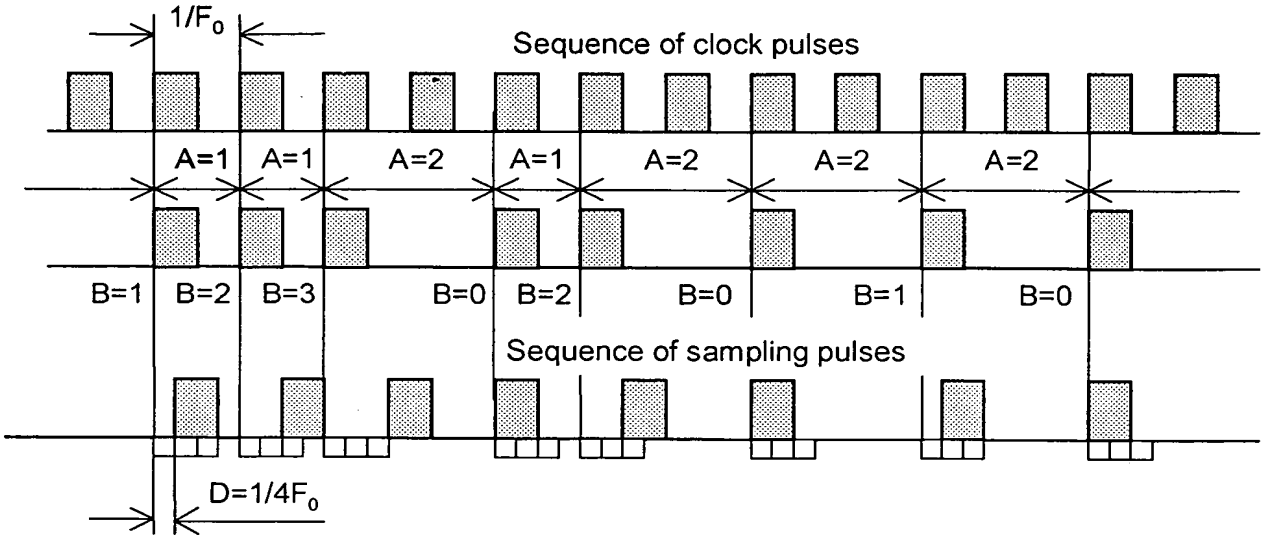

FIG.4. A time diagram showing the manner in which the sapling pulse sequence is adapted to the highest rate operation